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10/828,677	04/21/2004	Matthew A. Ahrens	03226.393001; P8512	4465

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HOUSTON, TX 77010

EXAMINER
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CAMPOS, YAIMA

ART UNIT	PAPER NUMBER
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2185

MAIL DATE	DELIVERY MODE
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06/29/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No. 10/828,677	Applicant(s) AHRENS ET AL.	
	Examiner Yaima Campos	Art Unit 2185	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 04 April 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>4/04/07</u> . | 6) <input type="checkbox"/> Other: _____  |

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### **DETAILED ACTION**

1. The instant application having Application No. 10/828,516 has a total of 23 claims pending in the application; there are 4 independent claims and 19 dependent claims, all of which are ready for examination by the examiner.

#### ***Continued Examination Under 37 CFR 1.114***

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 4, 2007 has been entered.

### **ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT**

3. As required by **M.P.E.P. 609(C)**, the applicant's submission of the Information Disclosure Statement dated May 12, 2006 are acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

### **REJECTIONS BASED ON PRIOR ART**

#### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. **Claims 1-11 and 13-22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Talangala et al. (US 2002/0161972) in view of Talagala et al. (US 2004/0024963), Dalal et al. (US 2004/0123063) and Lu et al. (Us 2004/0225834).

6. As per **claims 1, 13 and 21-22**, Talangala discloses

“A method/system/network system having a plurality of nodes for dynamic striping, comprising:” as [**“dynamic striping may be employed so that new writes form new parity group. Thus, stripes of various sizes may be supported by the storage system” (Column 2, paragraph 0012)**]

“software instructions stored in the memory for enabling the under control of the processor, to:” [**With respect to this limitation, Talangala discloses “To facilitate keeping track of the data and parity information, a block remapping technique may be implemented in software and/or hardware which maps a logical or virtual block address to a physical storage device segment” (Column 6, paragraph 0054 and Column 3, paragraph 0033, lines 21-26)**]

“receiving a request to write a **first** data block into a storage pool;” [**With respect to this limitation, Talangala discloses “receiving a write transaction specifying the virtual addresses of a subset of the data blocks of a data stripe” (Column 3, paragraph 0017 and Column 6, paragraph 0059)**]

“determining a physical disk location in the storage pool to store the **first** data block using a dynamic striping policy, **wherein the dynamic striping policy comprises at least one selected**

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from the group consisting of a dynamic striping policy based on physical disk speed, a dynamic striping policy based on free space available on physical disks, a dynamic striping policy based on load on physical disks, and a round robin policy;" [With respect to this limitation, Talangala discloses that "With dynamic striping, the host machine interacts with the storage array via virtual addresses" and explains that "When a block is written, a physical location is chosen for it" (Column 6, paragraph 0059). Talangala also discloses having a "free segment bitmap" used to "keep track of all physical segments on all storage devices" to allocate new data to free/empty segments (Column 5, paragraph 0051). Talagala also explains "when processor 100 of FIG. 1 write new data to array of storage devices 410 of FIG. 4, the data is again striped across the storage devices... the data blocks B(0) through B(3) and P(3) are stored across the storage devices such that the data and parity blocks are not stored on the same device... to reconstruct data in the event of a device failure, the blocks of new data that comprise a data stripe may be stored in locations on different devices" (Page 4, Par. 0043-Page 5, Par. 0045; Figure 4 and related text) which comprises "round-robin" between devices. Furthermore, "Fig. 5C illustrates an embodiment of how storage controller 401 of Fig. 3 may periodically realign non-uniformly sized parity groups into default sized parity groups" (Page 5, Par. 0046)]

"storing the **first** data block at the physical disk location; and storing a first indirect block in the storage pool using the dynamic striping policy, wherein the first indirect block comprises the **first** data block location and the **first** data block checksum" [Talangala discloses this limitation as "An indirection map (e.g. block remapping table) matches virtual block addresses to physical block addresses. Block-level checksums may be provided in the indirection map"

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(Column 6, paragraph 0059 and Figure 6C). Talagala also discloses “a checksum for each block may be stored as part of each block (e.g. amended to the end of each block) or stored at a separate disk location, memory table, etc... Therefore, block-level checksums may be stored in a separate physical locations from the blocks” (Page 6, Par. 0058) wherein “the indirection map (e.g. hashed indirection table and parity group table) may be separately stored on disk, cached, or stored in memory” (Page 7, Par. 0062)]

a first data block; a first indirect block; a parent block referencing the first indirect block, wherein the first indirect block references the first data block and comprises the first data block location and the first data block checksum; [Talagala discloses “an indirection map

(e.g., block remapping table) matches virtual block address to physical block address.

Block-level checksums may be provided in the indirection map” (Page 6, Par. 0059 and Figure 6C); “each valid PGT entry also includes a back pointer to the next entry in a parity group so that the first physical segment in a parity group is linked to a second physical segment in that parity group, and the second physical segment to the third and so on, until the last physical segment contains the parity data for that parity group. The physical segment that contains the parity data is linked back to the first physical segment in the parity group, thereby creating a circular list for that parity group” (Page 6, Par. 0056; Figure 6 and related text); [“Storage Controller 401” (Figures 2 and 3 and Column 3, paragraph 0033)]

“changing the dynamic striping policy to obtain an updated dynamic striping policy; and storing a second data block using the updated dynamic striping policy [ With respect to this limitation, Talagala discloses “dynamic striping may be employed so that new writes form new parity

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**groups. Thus, stripes of various sizes may be supported by the storage system” (Page 2, Par. 0012); therefore, updating the dynamic striping policy for new writes].**

Talagala (US 2002/0161972) does not disclose expressly specifically storing indirect blocks comprising data block location and data block checksum using data striping and does not specifically disclose the details having dynamic striping based on physical disk speed, free space available on physical disks, load on physical disks, and a round robin policy.

Talagala (US 2004/0024963) discloses storing indirect blocks comprising data block location and data block checksum using data striping as **[a “data layout architecture, and more specifically, to data layout architecture for storing and accessing integrity metadata” (Page 1, Par. 0002) “integrity metadata may include address data to verify the location of the data stripe unit, or a checksum to verify the contents of a data stripe unit” (Page 1, Par. 0006) “data striping to accommodate integrity metadata (IMD)... Data layout mechanism may include an array of G storage devices (e.g., disk drives) to accommodate stripes of data stripe units. Storage spaces may be allocated within each disk drive to store data stripe units and metadata chunks” (Page 2, Par. 0028) “the metadata chunks M1 through M7 are evenly distributed access the disk drives 202 through 208” (Page 2, Par. 0031) “FIGS. 6A through 6C illustrate operations of allocating IMD chunks within an array of disks employing data striping according to one embodiment of the present invention” (Page 3, Par. 0040)].**

To further support Talagala (US 2002/0161972) and Talagala (US 2004/0024963), Lu explicitly discloses updating a striping/storage policy as **[a system and method for optimizing storage operations in which “an archive manager is a computer program that manages**

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**archive operations, such as creating and updating a storage policy, and retrieving data related to a storage policy... details of storage policies, such as the copy name, data stream, media group, combine data stream properties, etc.” (Page 4, Par. 0046)].**

Dalal explicitly discloses a dynamic striping policy comprising at least one of a dynamic striping policy based on physical disk speed, free space available on physical disks, load on physical disks, and a round robin policy as [“**Allocation coordinator 1010 obtains data form configuration database 1004, which includes data about templates, capabilities, rules and policy database 1006, which contains information about storage environment policies. An example of a policy is a specification of a stripe unit width for creating columns in a striped virtual object” and explains that “allocation coordinator 1010 also obtains information about the available storage environment from storage information collector” (Column 6, paragraph 0102 and Column 12, paragraph 0187) as having rules to allocate storage based on available storage space. Dalal also teaches that “striped storage has capacity, maximum bandwidth, and maximum I/O rate that is the sum of the corresponding values of its constituent disks” (Columns 13-14, paragraph 0213) wherein “optimum stripe unit size must be determined on a case-by-case basis, taking into account access patterns presented by the applications that will use striped storage” (Column 14, paragraph 0215) as taking into account, storage capacity, bandwidth and I/O rate to stripe storage devices].**

Talangala et al. (US 2002/0161972), Talagala et al. (US 2004/0024963), Dalal et al. (US 2004/0123063) and Lu et al. (Us 2004/0225834) are analogous art because they are from the same field of endeavor of computer memory access and control.



At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the dynamic striping system as taught by Talangala (US 2002/0161972), and store metadata information such as location and checksum for every data block which Talagala (US 2002/0161972) stores within indirection map within metablocks as taught by Talaga (US 2004/0024963), and store these metablocks using striping or dynamic striping techniques as taught by Talagala (US 2004/0024963), further update a storage/striping policy as taught by Lu, and further stripe storage devices by selecting rules as taught by Dalal.

The motivation for doing so would have been because Talagala (US 2004/0024963) discloses storing metadata information such as location and checksum for every data block within metablocks is done to **[address the problem of data corruption (Page 1, Par. 0006)]** and storing these metablocks using striping or dynamic striping techniques is done to **[reduce the capacity overhead consumed by metadata arrangements (Pages 2-3, Par. 0031) and explains “it should be noted that the methods and data layout mechanisms taught by the present invention for providing extended data striping to accommodate integrity metadata may be implemented in any type of storage systems utilizing data striping” (Page 5, Par. 0057)]**. Dalal teaches that using certain rules to stripe a storage device **[“enable the device to provide certain capabilities, such as high performance, inherently” and explains that “to ensure that logical volume meets user requirements, a combination of physical characteristics of some storage devices and software configuration of other storage devices using rules can be used to provide all capabilities meeting the user requirements” (Column 6, paragraph 0100)]** and Lu teaches updating of striping/storage policies is done for **[“increasing the efficiency of storage management systems” (Page 2, Par. 0020)]**.

Therefore, it would have been obvious to combine Talangala et al. (US 2002/0161972) with Talagala et al. (US 2004/0024963), Dalal et al. (US 2004/0123063) and Lu et al. (US 2004/0225834) and for the benefit of creating a system/method for dynamic striping to obtain the invention as specified in claims 1 and 21.

7. As per **claim 2**, the combination of Talagala (US 2002/0161972), Talagala et al. (US 2004/0024963), Lu and Dalal discloses “The method of claim 1,” [See rejection to claim 1 above] “further comprising: retrieving the **first** data block using the first indirect block” [With respect to this limitation, Talangala disclose that “when a block read is requested, the block’s indirection map entry is read to find the block’s physical address” (Column 7, paragraph 0061, lines 8-10)].

8. As per **claim 3**, the combination of Talagala (US 2002/0161972), Talagala et al. (US 2004/0024963), Lu and Dalal discloses “The method of claim 1,” [See rejection to claim 1 above] “further comprising: assembling the first indirect block, wherein assembling the first indirect block comprises populating a block pointer” [Talangala discloses this concept as “a hash indirection table (HIT)” which “maps virtual block addresses to an entry or index number in a parity group table” (Column 6, paragraphs 0054-0055 and Figures 6B, 7A, 8A, 6C, 7B and 8B). Note that each virtual address in “HIT” maps to an entry in “PGT (parity group table)” and that each field in PGT table stores configuration information for each “indirect block”].

9. As per **claim 4**, the combination of Talagala (US 2002/0161972), Talagala et al. (US 2004/0024963), Lu and Dalal discloses “The method of claim 3,” [See rejection to claim 3 above] “wherein populating the block pointer comprises: storing the **first** data block checksum

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in a checksum field within the block pointer;” [Talangala discloses this concept as “each block’s checksum is stored in an entry in the indirection map, e.g. as part of a block remapping table entry (e.g. PGT entry) for each block” (Column 6, paragraph 0058, lines 4-6 and Figures 6C, 7B and 8B) wherein each entry representing/pointing to a block in PGT contains a checksum in a checksum field]

“and storing the first data block location in the block pointer, wherein storing the data block location comprises storing a metaslab ID” [Talangala discloses this concept as “the indirection map may also include a parity group pointer for each data block that points to a next member of that parity group” (Page 2, Par. 0013) wherein “when a READ or WRITE command is received for a block(s), the appropriate PGT entry is accessed to locate the blocks in the disk drives” (Page 6, Par. 0058) “HIT (Hash Indirection Table)” and explains having “PGT (Parity Group Table)” indices to access a PGT which contains configuration information for each of the parity groups such as a segment field which indicated the physical disk location (disk and segment) of parity groups (Column 6, paragraphs 0055, 0058, 0059 and Figures 6B, 6C, 7A, 7B, 8A and 8B). Talangala provides an example in which Virtual address 0 corresponds to PGT index 12, which contains valid data at physical segment D1.132 wherein “this may be interpreted as Disk 1, segment 132” (Column 6, paragraph 0057 and Figures 6B, 6C, 7A, 7B, 8A and 8B). As defined by Applicant, metaslabs are “contiguous regions of data” in which “the storage space in the storage pool is divided” (Specification, Par. 0031); therefore, Applicant should note that these metaslabs may comprise any amount of contiguous data, such as segments or blocks into which a storage pool is divided, as described by Talagala]

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“and offset” [Talagala discloses this concept as entries stored under the “Next Entry In Parity Group” field in PGT (parity group table) which points to the next virtual block entry (Column 6, paragraph 0057 and Figures 6B, 6C, 7A, 7B, 8A and 8B)].

10. As per claim 5, the combination of Talagala (US 2002/0161972), Talagala et al. (US 2004/0024963), Lu and Dalal discloses “The method of claim 4,” [See rejection to claim 4 above] “further comprising: storing a birth value in a birth field within the block pointer” [Talagala discloses this concept as an embodiment having a “HIT (hash indirection table) which maintains generational images” and explains that “the PGT index columns are now labeled version zero through version two, where version zero corresponds to the most current version and version two corresponds to the oldest version” (Column 7, paragraph 0065 and Figures 8A and 8B)].

11. As per claims 6 and 15, the combination of Talagala (US 2002/0161972), Talagala et al. (US 2004/0024963), Lu and Dalal discloses “The method/system of claims 3 and 13,” [See rejection to claim 3 and 13 above] “wherein the first indirect block is assembled using a data management unit” [With respect to this limitation, Talagala discloses “Storage Controller 401” (Figures 2 and 3 and Column 3, paragraph 0033)].

12. As per claims 7 and 17, the combination of Talagala (US 2002/0161972), Talagala et al. (US 2004/0024963), Lu and Dalal discloses “The method/system of claims 1 and 13,” [See rejection to claims 1 and 13 above] “wherein the storage pool comprises at least one storage device” [With respect to this limitation, Talagala discloses “Array of Storage Devices 410” (Figures 2 and 3)].

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13. As per claims 8 and 18, the combination of Talagala (US 2002/0161972), Talagala et al. (US 2004/0024963), Lu and Dalal discloses “The method/system of claims 1 and 13,” [See rejection to claims 1 and 13 above] “wherein the storage pool is divided into a plurality of metaslabs” [With respect to this limitation, Talangala discloses having different “stripes of data” within an array storage devices (Figure 4 and Column 4, paragraph 0043) and explains that a “stripe” of data is analogous to a “parity group” (Column 7, paragraph 0063, lines 10-11) wherein configuration information for each of the “parity groups” is stored in a “PGT (parity group table)” (Figures 6C, 7B and 8B) and further explains “the indirection map may also include a parity group pointer for each data block that points to a next member of that parity group” (Page 2, Par. 0013) wherein “when a READ or WRITE command is received for a block(s), the appropriate PGT entry is accessed to locate the blocks in the disk drives” (Page 6, Par. 0058). As defined by Applicant, metaslabs are “contiguous regions of data” in which “the storage space in the storage pool is divided” (Specification, Par. 0031); therefore, Applicant should note that these metaslabs may comprise any amount of contiguous data, such as segments or blocks into which a storage pool is divided, as described by Talagala].

14. As per claims 9 and 19, the combination of Talagala (US 2002/0161972), Talagala et al. (US 2004/0024963), Lu and Dalal discloses “The method/system of claims 8 and 18,” [See rejection to claims 8 and 18 above] “wherein each of the plurality of metaslabs is associated with a metaslab ID” [Talangala discloses this concept as each virtual block has a virtual address which is used to access a “HIT (Hash Indirection Table)” which contains “PGT (Parity Group Table)” indices to access a PGT which contains configuration information

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for each of the parity groups such as a segment field which indicated the physical disk location (disk and segment) of parity groups (Column 6, paragraphs 0055, 0058, 0059 and Figures 6B, 6C, 7A, 7B, 8A and 8B)].

15. As per claims 10 and 20, the combination of Talagala (US 2002/0161972), Talagala et al. (US 2004/0024963), Lu and Dalal discloses “The method of claims 9 and 19,” [See rejection to claims 9 and 19 above] “wherein the data block location comprises the metaslab ID and an offset” [Talagala discloses this concept as “the indirection map may also include a parity group pointer for each data block that points to a next member of that parity group” (Page 2, Par. 0013) wherein “when a READ or WRITE command is received for a block(s), the appropriate PGT entry is accessed to locate the blocks in the disk drives” (Page 6, Par. 0058) “HIT (Hash Indirection Table)” and explains having “PGT (Parity Group Table)” indices to access a PGT which contains configuration information for each of the parity groups such as a segment field which indicated the physical disk location (disk and segment) of parity groups (Column 6, paragraphs 0055, 0058, 0059 and Figures 6B, 6C, 7A, 7B, 8A and 8B). Talagala provides an example in which Virtual address 0 corresponds to PGT index 12, which contains valid data at physical segment D1.132 wherein “this may be interpreted as Disk 1, segment 132” (Column 6, paragraph 0057 and Figures 6B, 6C, 7A, 7B, 8A and 8B). As defined by Applicant, metaslabs are “contiguous regions of data” in which “the storage space in the storage pool is divided” (Specification, Par. 0031); therefore, Applicant should note that these metaslabs may comprise any amount of contiguous data, such as segments or blocks into which a storage pool is divided, as described by Talagala (US 2002/0161972)]

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“and offset” [Talagala discloses this concept as entries stored under the “Next Entry In Parity Group” field in PGT (parity group table) which points to the next virtual block entry (Column 6, paragraph 0057 and Figures 6B, 6C, 7A, 7B, 8A and 8B)]

16. As per claim 11, the combination of Talagala (US 2002/0161972), Talagala et al. (US 2004/0024963), Lu and Dalal discloses “The method of claim 1,” [See rejection to claim 1 above] “wherein storing the first data block comprises using a storage pool allocator” [With respect to this limitation, Talagala discloses “Storage Controller 401” (Figures 2 and 3 and Column 3, paragraph 0033)].

17. As per claim 14, the combination of Talagala (US 2002/0161972), Talagala et al. (US 2004/0024963), Lu and Dalal discloses “The system of claim 13,” [See rejection to claim 13 above] “further comprising: a second indirect block, comprising a first indirect block checksum and a first indirect block location, wherein the storage pool allocator is further configured to store the second indirect block in the storage pool” [With respect to this limitation, Talagala discloses writing a block having a checksum and a location in PGT (Parity Group Table) which have a “segment” field to store a location and a “checksum” field to store a checksum (Column 6, paragraph 0059 and Figures 6C, 7B and 8B) and provides (Figures 6C, 7B and 8B) which contain parity/stripe group tables having entries for multiple blocks of data stored in a storage pool].

18. As per claim 16, the combination of Talagala (US 2002/0161972), Talagala et al. (US 2004/0024963), Lu and Dalal discloses the system of claims 13, wherein the dynamic striping policy comprises at least one selected from the group consisting of a dynamic striping policy based on physical disk speed, a dynamic striping policy based on free space available on physical

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disks, a dynamic striping policy based on physical disks, and a round robin policy [The rationale in the rejection to claims 1 and 21 is herein incorporated].

#### **ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT**

##### **Response to Amendment**

19. Applicant's arguments filed April 4, 2007 have been fully considered but they are moot in view of new grounds of rejection.

20. As required by M.P.E.P. § 707.07(f), a response to these arguments appears below.

#### **ARGUMENTS CONCERNING PRIOR ART REJECTIONS**

21. Claims must be given the broadest reasonable interpretation during examination and limitations appearing in the specification but not recited in the claim are not read into the claim (See M.P.E.P. 2111 [R-1]).

22. All arguments by the applicant are believed to be covered in the body of the office action or in the above remarks and thus, this action constitutes a complete response to the issues raised in the remarks dated April 4, 2007.

#### **CLOSING COMMENTS**

##### **Examiner's Note**

23. Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the



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individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

**Conclusion**

**a. STATUS OF CLAIMS IN THE APPLICATION**

24. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. 707.07(i):

**a(1) CLAIMS REJECTED IN THE APPLICATION**

25. Per the instant office action, claims 1-22 have received a first action on the merits and are subject of a first action non-final.

**b. DIRECTION OF FUTURE CORRESPONDENCES**

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

**IMPORTANT NOTE**

27. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

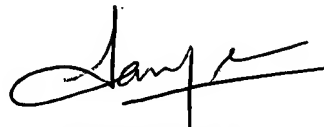
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The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 15, 2007



Yaima Campos  
Examiner  
Art Unit 2185



**SANJIV SHAH**  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100